Exhibit 4

Claims Reciting A "Encoded" PCI Bus Transaction Or A PCI Bus Transaction In "Serial Stream" Or "Serial Form"

Claim Limitations	Asserted Claims
"**encoded** address and data bits of a Peripheral Component Interconnect (PCI) bus transaction in (a) **serial** form/bit stream"	'768 patent, claims 4, 7, 18, 30, 39; '750 patent, claims 5, 10, 14, 35, 46; '797 patent, claims 7, 10, 14, 36; '977 patent, claims 1, 9, 10, 16; '654 patent, claim 14.
"**encoded** address bits, data bits, and byte enable information bits of a Peripheral Component Interconnect (PCI) bus transaction in **serial** form"	'750 patent, claims 18, 21, 27, 44.
"**encoded serial** bit stream of address bits, data bits, and byte enable information bits of (a) PCI bus transaction"	'947 patent, claims 35, 48, 51.
"**encoded serial** bit stream of (encoded) address and data bits of a Peripheral Component Interconnect (PCI) bus transaction"	'739 patent, claims 29, 31; '468 patent, claims 14, 26, 29, 35, 37, 45; '947 patent, claims 54, 57.
"**encoded serial** bit stream of Peripheral Component Interconnect (PCI) bus transaction"	'624 patent, claim 6; '873 patent, claims 54, 77, 97; '984 patent, claim 52.
"**encoded** address and data bits of a Peripheral Component Interconnect (PCI) bus transaction with **different serialized forms**"	'768 patent, claim 8.
"**encoded** address and data (bits) of a Peripheral Component Interconnect (PCI) bus transaction"	'768 patent, claims 9, 22, 33; '140 patent, claim 30.
"**encoded** Peripheral Component Interconnect (PCI) address and data bits of a PCI bus transaction"	'359 patent, claims 3, 7, 17.
"**encoded** PCI bus transaction data"	'624 patent, claim 11.